FIG. 1

RTL
LOGIC DESCRIPTION — 1

↓

RTL DESCRIPTION
INPUTTING MEANS — 3

↓

SYNTAX ANALYZING
MEANS — 4

↓

INVARIABLE ATTRIBUTE
SETTING MEANS — 5

↓

2

LIBRARY

PARTIAL CIRCUIT
SYNTHESIZING MEANS — 6

↓

INVARIABLE PART
OPTIMIZING MEANS — 7

↓

PERFORMANCE
CALCULATING MEANS — 8

↓

DISPLAY MEANS — 9

FIG. 2A

```
wire [7:0] A,B,Y;
wire sel;
...
assign Y = (sel==1'b1)?A+B:A;
```

FIG. 2B

signal	file	line
A[7:0]	design1.v	50
B[7:0]	design1.v	60
Y[7:0]	design1.v	70
sel	design1.v	65

FIG. 2C

F I G. 3

20 IS THERE UNPROCESSED SIGNAL HAVING INVARIABLE ATTRIBUTE? — No → END

Yes

21 SELECT ONE OF SIGNALS HAVING INVARIABLE ATTRIBUTES

Yes ← **22** IS NUMBER FO OF FAN-OUTS OF SIGNAL DESIGN RULE N OR LESS?

No

23 DIVIDE DEVICES RECEIVING SIGNALS AS INPUTS INTO FO/N NUMBER OF AGGREGATIONS

24 INSERT BUFFER INTO SIGNAL IN SUCH MANNER AS TO CONNECT ALL OF DEVICES IN EACH OF AGGREGATIONS
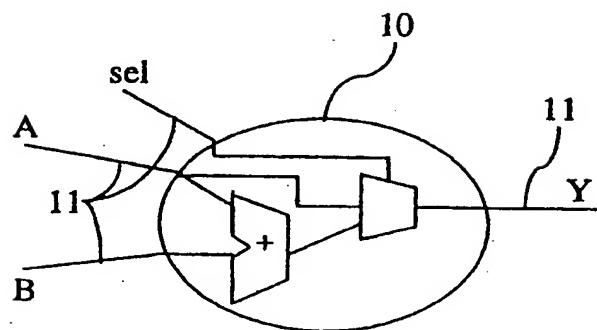
F I G. 4A

Module xxx
Area : 10000
Max Delay 10.5

F I G. 4B

from	to	delay
block1/rega	block2/regb	9.4
block2/regb	block2/regc	5.6
block2/regc	block3/regd	10.4

F I G. 4C

Y:delay
4nscc
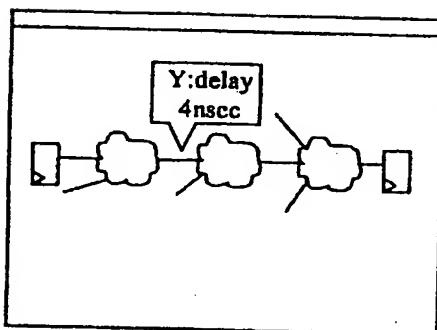
F I G. 4D

```
always @(A or B or C or D) begin
   if (D==1'b0) begin
      Y=A + B;
   end
   else begin
      Y=A + C;
   end
end
```

F I G. 5A

```
always @(A or B or C or D) begin
  if (D==1'b0) begin
    Y=A + B;
  end
  else begin
    Y=A + C;
  end
end
```

F I G. 5B
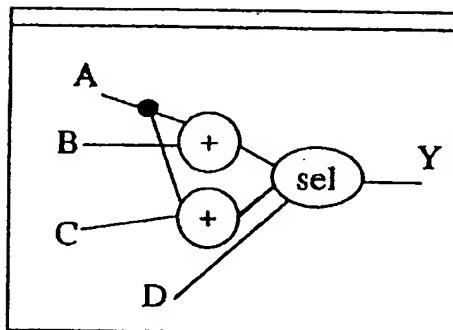
F I G. 5C

Signal	arrival
A	3.5
B	2.6
C	2.8
D	2.0
Y	9.6

F I G. 5D

Signal	arrival
A	3.5
B	2.6
C	2.8
D	4.0
Y	9.6

FIG. 6A

```
always @(A or B or C or D) begin
   if (D==1'b0) begin
      Z=B;
   end
   else begin
      Z=C;
   end
   Y=A+Z;
end
```

FIG. 6B
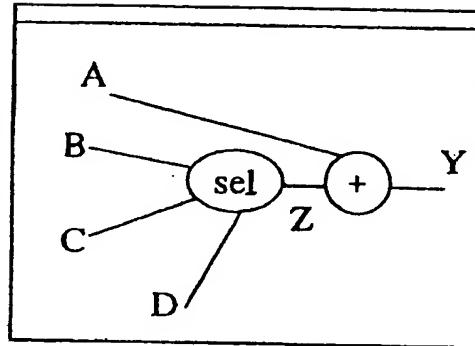
FIG. 6C

Signal	arrival
A	3.5
B	2.6
C	2.8
D	2.0
Y	8.9

FIG. 6D

Signal	arrival
A	3.5
B	2.6
C	2.8
D	4.0
Y	10.1

FIG. 7

RTL
LOGIC DESCRIPTION — 1

↓

RTL DESCRIPTION
INPUTTING MEANS — 3

↓

SYNTAX ANALYZING MEANS — 4

↓

INVARIABLE ATTRIBUTE
SETTING MEANS — 5

↓

PARTIAL CIRCUIT
SYNTHESIZING MEANS — 6

↓

FLOORPLAN MEANS — 30

↓

INVARIABLE PART OPTIMIZING
MEANS — 7

↓

FLOORPLAN UPDATING
MEANS — 31

↓

INTERCONNECT PREDICTING
MEANS — 32

↓

PERFORMANCE CALCULATING
MEANS — 8

↓

DISPLAY MEANS — 9

2

LIBRARY

FIG. 8

SET ARRANGEMENT REGION — 40

ARRANGE IO — 41

HIERARCHICAL LAYOUT? — 42

No

CREATE GROUP — 43

ARRANGE GROUP — 44

ARRANGE DEVICE INSIDE OF GROUP — 45

Yes

DIVIDE BLOCK — 46

ARRANGE BLOCK — 47

ARRANGE BLOCK PIN — 48

ARRANGEMENT INSIDE OF BLOCK

CREATE GROUP

ARRANGE GROUP — 49

ARRANGE DEVICE INSIDE OF GROUP

F I G. 9

F I G. 10

RTL
LOGIC DESCRIPTION — 1

2

LIBRARY

RTL PERFORMANCE
ESTIMATING MEANS — 50

DISPLAY
MEANS — 9

DELAY RECALCULATING
MEANS

51

FIG. 11A

52   52   52

FIG. 11B